

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Previously Amended) A digital system, comprising:
2 a memory circuit;
3 a first requestor circuit with a first memory access node;
4 a second requestor circuit with a second memory access node;
5 a scheduling circuit connected to the first memory access node
6 and to the second memory access node and having a request output
7 node, operable to sequentially schedule memory accesses to the
8 memory circuit by the first requestor circuit and by the second
9 request circuit;
10 a selection circuit connected to the first memory access node
11 and to the scheduling circuit request output node with an output
12 node connected to the memory circuit;
13 access mode circuitry for indicating at least a first access
14 mode and a second access mode controllably connected to the
15 selection circuit, such that both the first requestor circuit and
16 the second requestor circuit can sequentially access the memory
17 circuit when the access mode circuitry indicates the first access
18 mode and the first requestor circuit has exclusive access to the
19 memory circuit when the access mode circuitry indicates the second
20 access mode; and
21 a size register for holding a size parameter coupled to the
22 selection circuit, the selection circuit being operable to select a
23 first portion of the memory circuit in response to the size
24 parameter when the access mode circuitry indicates the second
25 access mode, wherein only the first portion of the memory circuit
26 is operable for exclusive access by the first requestor when the
27 access mode circuitry indicates the second access mode.

1 2. (Original) The digital system of Claim 1, wherein a
2 second portion of the memory circuit not selected in response to
3 the size parameter is operable to be in a low power mode when the
4 access mode circuitry indicates the second access mode.

1 3. (Original) The digital system according to Claim 1,
2 wherein the selector circuit is operable such that a second portion
3 of the memory circuit not selected in response to the size
4 parameter can be accessed by the second requestor when the access
5 mode circuitry indicates the second access mode.

1 4. (Original) The digital system according to Claim 1,
2 wherein the size parameter is ignored when the access mode
3 circuitry indicates the first access mode such that the entire
4 memory circuit is operable to be selected for sequential access by
5 the first requestor and the second requestor.

1 5. (Currently Amended) ~~The A~~ digital system ~~according to~~
2 ~~Claim 1, further~~ comprising:
3 a memory circuit;
4 a first requestor circuit with a first memory access node;
5 a second requestor circuit with a second memory access node;
6 a scheduling circuit connected to the first memory access node
7 and to the second memory access node and having a request output
8 node, operable to sequentially schedule memory accesses to the
9 memory circuit by the first requestor circuit and by the second
10 request circuit;
11 a selection circuit connected to the first memory access node
12 and to the scheduling circuit request output node with an output
13 node connected to the memory circuit;

14 access mode circuitry for indicating at least a first access
15 mode and a second access mode controllably connected to the
16 selection circuit, such that both the first requestor circuit and
17 the second requestor circuit can sequentially access the memory
18 circuit when the access mode circuitry indicates the first access
19 mode and the first requestor circuit has exclusive access to the
20 memory circuit when the access mode circuitry indicates the second
21 access mode;

22 a size register for holding a size parameter coupled to the
23 selection circuit, the selection circuit being operable to select a
24 first portion of the memory circuit in response to the size
25 parameter when the access mode circuitry indicates the second
26 access mode, wherein only the first portion of the memory circuit
27 is operable for exclusive access by the first requestor when the
28 access mode circuitry indicates the second access mode; and

29 a clock circuit connected to the second requestor and to the
30 memory circuit, wherein the first portion of the memory circuit
31 operates synchronously with the clock circuit when the access mode
32 circuitry indicates the first access mode and wherein the first
33 portion of the memory circuit operates in an asynchronous manner
34 when the access mode circuitry indicates the second access mode.

1 6. (Original) The digital system according to Claim 1,
2 wherein the first requester circuit is a host processor and the
3 second requester circuit is direct memory access circuit channel
4 controller.

7. (Canceled)

1 8. (Original) A method of operating a digital system having
2 a memory circuit that is shared by a plurality of requestor
3 circuits, comprising the steps of:

4 sharing access to the memory circuit between the plurality of
5 requestor circuits when the digital system is in a first mode of
6 operation;

7 selecting a first portion of the memory circuit responsive to
8 a size parameter stored in a register, such that a second portion
9 of the memory circuit is not selected; and

10 limiting access to the first portion of memory circuit to only
11 a first requestor of the plurality of requestors when the digital
12 system is in a second mode of operation.

1 9. (Original) The method of Claim 8, further comprising the
2 step of sharing access to the second portion of the memory circuit
3 between the plurality of requestor circuits when the digital system
4 is in the second mode of operation.

1 10. (Original) The method of Claim 8, further comprising the
2 step of placing the second portion of the memory circuit in a low
3 power mode when the digital system is in the second mode of
4 operation.

1 11. (Previously Added) The method of Claim 8, wherein the
2 memory has a total size equal to the sum of the first portion and
3 the second portion.

1 12. (Previously Added) The method of Claim 11, further
2 comprising the step of storing a different size parameter in the
3 register, such that the step of selecting results in a first

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4 portion having a different size in response to the different size
5 parameter.
